AMENDMENTS TO THE CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. (Currently Amended) A pixel cell comprising:

a photo-conversion device;

a storage node switchably coupled to the photo-conversion device for receiving charge from the photo-conversion device via a shutter transistor[[,]];

a capacitor electrically connected to a gate of the shutter transistor and the storage node;

a sensing node switchably coupled to the storage node for receiving the charge from the storage node; and

an anti-blooming circuit electrically connected to the photo-conversion device for selectively draining charge from the photo-conversion device.

2. (Original) The pixel cell of claim 1, further comprising a readout and reset circuit electrically connected to the sensing node to output the charge accumulated at the sensing node.

3. (Original) The pixel cell of claim 2, wherein the readout and reset circuit comprises:

a reset transistor electrically connected to the sensing node;

a source-follower transistor, wherein the source follower transistor comprises a gate, wherein the source follower gate is electrically connected to the sensing node; and

a row select transistor electrically connected to the source-follower transistor.

4. (Original) The pixel cell of claim 3, wherein at least one of the sensing node, reset transistor, source follower transistor, and row select transistor are shared with at least one other pixel cell.

5. (Currently amended) The pixel cell of claim 3, wherein the anti-blooming circuit, reset transistor, and source follower transistor are electrically connected to a common voltage source.

6. (Original) The pixel cell of claim 1, wherein the photo-conversion device is a pinned photodiode.

7. (Original) The pixel cell of claim 1, wherein the sensing node is a floating diffusion node.

8. (Original) The pixel cell of claim 1, wherein the anti-blooming circuit is an anti-blooming transistor.

9. (Original) The pixel cell of claim 8, wherein the sensing node is switchably coupled to the storage node by a transfer transistor, wherein the transfer transistor and the anti-blooming transistor each comprise respective gates, and wherein the gate of the anti-blooming transistor is electrically connected to the gate of the transfer transistor.

10. (Original) The pixel cell of claim 1, wherein the sensing node is switchably coupled to the storage node by a transfer transistor.

11. (Original) The pixel cell of claim 1, wherein the storage node is a doped region of a second conductivity type below a surface of a substrate.

12. (Original) The pixel cell of claim 1, wherein the capacitor is above a substrate.

13. (Original) The pixel cell of claim 1, wherein the capacitor is a polypropylene capacitor.

14. (Original) A pixel cell comprising:

a photo-conversion device;

a storage node switchably coupled to the photo-conversion device for receiving charge from the photo-conversion device via a shutter transistor, a gate of the shutter transistor being electrically connected to the storage node;

a first barrier region adjacent to the storage node, the barrier region being electrically connected to the gate of the shutter transistor;

a sensing node switchably coupled to the storage node for receiving the charge from the storage node; and

an anti-blooming circuit electrically connected to the photo-conversion device for selectively draining charge from the photo-conversion device.

15. (Original) The pixel cell of claim 14, further comprising a readout and reset circuit electrically connected to the sensing node to output the charge accumulated at the sensing node.

16. (Original) The pixel cell of claim 15, wherein the readout and reset circuit comprises:

a reset transistor electrically connected to the sensing node;

a source-follower transistor, wherein the source follower transistor comprises a gate, wherein the source follower gate is electrically connected to the sensing node; and

a row select transistor electrically connected to the source-follower transistor.

17. (Original) The pixel cell of claim 16, wherein at least one of the sensing node, reset transistor, source follower transistor, and row select transistor are shared with at least one other pixel cell.

18. (Currently Amended) The pixel cell of claim 16, wherein the anti-blooming circuit, reset transistor, and source follower transistor are electrically connected to a common voltage source.

19. (Original) The pixel cell of claim 14, wherein the photo-conversion device is a pinned photodiode.

20. (Original) The pixel cell of claim 14, wherein the sensing node is a floating diffusion node.

21. (Original) The pixel cell of claim 14, wherein the anti-blooming circuit is an anti-blooming transistor.

22. (Original) The pixel cell of claim 21, wherein the sensing node is switchably coupled to the storage node by a transfer transistor, wherein the transfer transistor and the anti-blooming transistor each comprise respective gates, and wherein the gate of the anti-blooming transistor is electrically connected to the gate of the transfer transistor.

23. (Original) The pixel cell of claim 14, wherein the sensing node is switchably coupled to the storage node by a transfer transistor.

24. (Original) The pixel cell of claim 14, wherein the storage node is a doped region of a second conductivity type below a surface of a substrate.

25. (Original) The pixel cell of claim 14, wherein the first barrier region is a heavily doped region of a first conductivity type below a surface of a substrate.

26. (Original) The pixel cell of claim 14, wherein the barrier region is between the photo-conversion device and the storage node.

27. (Original) The pixel cell of claim 14, further comprising a second barrier region between the barrier region and the sensing node.

28. (Original) The pixel cell of claim 27, wherein the second barrier region is a heavily doped region of a first conductivity type below a surface of a substrate.

29. (Original) A pixel sensor array comprising:

at least one subset of pixel cells at a surface of a substrate, the at least one subset comprising:

at least two photo-conversion devices;

at least two anti-blooming transistors, each anti-blooming transistor being electrically connected to a respective photo-conversion device for selectively draining charge from the respective photo-conversion device;

at least two storage nodes switchably coupled to a respective photo-conversion device for receiving charge from the respective photo-conversion device via a respective shutter transistor, a gate of each shutter transistor being electrically connected to a respective storage node; and

a sensing node switchably coupled to the storage nodes for receiving the charge from the storage nodes via respective transfer transistors, a gate of each transfer transistor being electrically connected to a respective gate of an anti-blooming transistor.

30. (Original) The array of claim 29, wherein the at least one subset of pixel cells further comprises a reset and readout circuit electrically connected to the sensing node.

31. (Original) The array of claim 30, wherein the reset and readout circuit comprises:

a reset transistor electrically connected to the floating diffusion node for resetting the voltage on the sensing node;

a source-follower transistor electrically connected to the reset transistor for receiving charge from the sensing node; and

a row select transistor electrically connected to the source-follower transistor for outputting a signal produced by the source follower transistor.

32. (Original) The array of claim 31, wherein the at least two anti-blooming transistors, the reset transistor, and the source follower transistor are electrically connected to a common voltage source.

33. (Original) The array of claim 29, wherein the sensing node is a floating diffusion node.

34. (Original) The array of claim 29, wherein the storage nodes are doped regions of a second conductivity type below the surface of the substrate.

35. (Original) The array of claim 29, wherein the at least one subset of pixel cells further comprise at least two barrier regions, each barrier region being between a respective photo-conversion device and a respective storage node, and wherein the barrier region is a doped region of a first conductivity type below a surface of the substrate.

36. (Original) The array of claim 29, wherein the at least one subset further comprises at least two capacitors, each capacitor electrically connected to a respective shutter gate and a respective storage node.

37. (Original) The array of claim 36, wherein the at least two capacitors are above the substrate.

38. (Original) The array of claim 36, wherein the at least two capacitors are polypropylene capacitors.

39. (Currently Amended) A processor-based system comprising:

a processor; and

an imager coupled to the processor, the imager comprising an array of pixel cells, at least one of the pixel cells comprising:

a photo-conversion device;

a storage node switchably coupled to the photo-conversion device for receiving charge from the photo-conversion device via a shutter transistor[[,]];

a capacitor electrically connected to a gate of the shutter transistor and the storage node;

a sensing node switchably coupled to the storage node for receiving the charge from the storage node; and

an anti-blooming circuit electrically connected to the photo-conversion device for selectively draining charge from the photo-conversion device.

40. (Original) A processor-based system comprising:

a processor; and

an imager coupled to the processor, the imager comprising an array of pixel cells, at least one of the pixel cells comprising:

a photo-conversion device;

a storage node switchably coupled to the photo-conversion device for receiving charge from the photo-conversion device via a shutter transistor, a gate of the shutter transistor being electrically connected to the storage node;

a first barrier region adjacent to the storage node, the barrier region being electrically connected to the gate of the shutter transistor;

a sensing node switchably coupled to the storage node for receiving the charge from the storage node;

a second barrier region between the storage node and the sensing node; and

an anti-blooming circuit electrically connected to the photo-conversion device for selectively draining charge from the photo-conversion device.

41. (Currently Amended) An integrated circuit comprising:

an array of pixel cells, each pixel cell comprising:

a photo-conversion device;

a storage node switchably coupled to the photo-conversion device for receiving charge from the photo-conversion device via a shutter transistor[[,]];

a capacitor electrically connected to a gate of the shutter transistor and the storage node;

a sensing node switchably coupled to the storage node for receiving the charge from the storage node; and

an anti-blooming circuit electrically connected to the photo-conversion device for selectively draining charge from the photo-conversion device.

42. (Original) The integrated circuit of claim 41, further comprising a readout and reset circuit electrically connected to the sensing node to output the charge accumulated at the sensing node.

43. (Original) The integrated circuit of claim 42, wherein the sensing node and readout and reset circuit are shared between at least two pixel cells of the array.

44. (Original) An integrated circuit comprising:

an array of pixel cells, each pixel cell comprising:

a photo-conversion device;

a storage node switchably coupled to the photo-conversion device for receiving charge from the photo-conversion device via a shutter transistor, a gate of the shutter transistor being electrically connected to the storage node;

a first barrier region adjacent to the storage node, the barrier region being electrically connected to the gate of the shutter transistor;

a sensing node switchably coupled to the storage node for receiving the charge from the storage node; and

an anti-blooming circuit electrically connected to the photo-conversion device for selectively draining charge from the photo-conversion device.

45. (Original) The integrated circuit of claim 44, further comprising a second barrier region between the storage node and the sensing node.

46. (Original) The integrated circuit of claim 44, further comprising a readout and reset circuit electrically connected to the sensing node to output the charge accumulated at the sensing node.

47. (Original) The integrated circuit of claim 46, wherein the sensing node and readout and reset circuit are shared between at least two pixel cells of the array.

48-60. (Cancelled)